Exhibit 24

Victor F Andrade · 3rd

IP Management

- Ambiq
- University of Pennsylvania

Austin, Texas, United States · Contact info

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About

• Proven technical leadership working with teams of highly skilled designers in the development of custom/semi-custom digital components, across many generations of AMD processors. Designs included memory arrays, SRAMs, ROMs, Register-File arrays and other custom specific IPs, including the base-cell components ...see more

Activity

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Victor F Andrade commented on a post • 2mo

A highly talented and experienced individual. Certainly, a very valuable asset at any company in our industry. Congratulations, Aulihan!

154 35 comments

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Experience

IP Management, Verification and Validation
Ambiq · Full-time
Jun 2022 - Present · 10 mos
Austin, Texas, United States

AMS Verification Manager
Mythic
May 2019 - Present · 3 yrs 11 mos
Austin, Texas Area

Principal Engineer/Manager
Qualcomm
Mar 2013 - Feb 2019 · 6 yrs
Austin, Texas Area

AMD
21 yrs 8 mos

PMTS, Chip Level Circuits Design Manager/Technical Lead.
Jun 2012 - Dec 2012 · 7 mos
Austin, Texas

Worked with and guided the team responsible for the design of the custom circuits used at the chip-level of AMD's recent 28nm APU devices. Team owned the custom IPs for the North-Bridge and GPU Clock-Control Units:

• North-Bridge SRAM 32K and 64K arrays.

• North-Bridge Register File Memory and Dual-Supply Port FIFO Array.

• Digital Clock-Synthesizer and Clock-Stretcher, based on manipulation of multi-phase outputs produced from the PLL and power domains droop-detection circuits.

• North-Bridge Clock Distribution network and building blocks

Circuit Methodology/Analysis Lead, 28nm APU Processor. PMTS.
Dec 2010 - May 2012 · 1 yr 6 mos
Austin, Texas

• Worked in the establishment of the macro design guidelines by working with a small team of tool owners to define consistent procedures in the functional, electrical and power integrity analysis and establish the design metrics, all based on Globalfoundries (GF) 28nm process parameters.

• Closely interacted with CAD team to propose tool enhancements, as well

- Closely interacted with CAD team to propose tool enhancements, as well as monitoring of pending bug fixes.

• Drove the initial timing analysis of a couple of custom IPs, Execution Unit Shifter-Array and Register-File macros using Synopsys's NanoTime tool.

• Developed Twiki Pages to automatically and periodically post guidelines and tracking of tool bugs. Among guidelines: Design-Topology, Beta-Ratio, Fanout/Sizing, Write-Ability, Cell-Stability, Noise Analysis, IR-drop limits, EM/FIT budget, Reliability, Dynamic and Static Patterns for Power Characterization, Timing Rules and Constraints, DFT, DFM, Multi-Clock/Power-Domain Crossing, Initialization, among others.

• Defined tape-out checklists to ensure full adherence of design guidelines to attain best margins and robust operation of our designs. Focused on the physical/construction, functional, electrical and long term reliability requirements.

• Created Twiki/HTML utility to automatically monitor checklist completion for each macro/IP component, held reviews until full closure of action items and final tape-out sign-off.

Design Manager/Technical Lead. PMTS.

May 2001 - Nov 2010 · 9 yrs 7 mos
Austin, Texas

Managed and provided technical guidance to a team of designers in the design and development of custom digital circuits for various generations of AMD Microprocessors. Actively involved in the initial planning; feasibility studies; milestone scheduling; driving and participating in circuit design reviews; functional and timing verification; variability/skewed-corner checks, establishment of design guidelines/checklists; team personnel administration and assessment reviews; coordinating the resolution of design issues or concerns with various support technical teams and IP consumer teams; silicon debug and bring-up; executive updates and progress reports; created HTML based scoreboard to automatically track and report the electrical and functional analysis results for each IP; silicon debug liaison with process and product teams; among other activities for the following processor developments:

- Llano/Husky APU Processor, GF's 32nm Process.
- Cell-base designs for compiled arrays, 45nm/32nm Fabs.
- Ridgeback CPU Processor, GF's 45nm Process.
- Barcelona CPU Processor. AMD's 65nm Fab.
- 65nm Test-Chip. AMD's Dresden Fab bring-up.
- K9 CPU. AMD's 90nm Fab.

Show all 6 experiences →

Senior Design Engineer
Commodore Business Machines, Inc
May 1984 - Apr 1991 · 7 yrs
West Chester, PA

Main circuit designer of the Video Controllers (DMA, UART and other microcontrollers) for the VIC20, Commodore C64, C128, C65 and Amiga...

Show all 11 experiences →

Education

University of Pennsylvania
Master of Science, Electrical Engineering
1985 - 1988

University of Pennsylvania
Bachelor of Science, Electrical Engineering
1977 - 1981

Activities and societies: Tau Beta Pi, Eta Kappa Nu.

Skills

SoC
33 endorsements

Physical Design
Endorsed by Scott Johnson and 1 other who is highly skilled at this

Endorsed by 23 colleagues at AMD

24 endorsements

ASIC
25 endorsements

Show all 16 skills →

Recommendations

Received Given

Tom Meneghini · 3rd
Principal Member of Technical Staff at AMD
March 25, 2013, Victor F was senior to Tom but didn't manage Tom directly

Over the course of the Steamroller project I had opportunity to interact with Victor on a number of occasions. Each time I was impressed by his depth of knowledge, understanding of the big picture, and interpersonal skills. Victor is an accomplished manager and technical lead who is respected and...

Publications

An x86 64 core implemented in 32nm SOI CMOS.

IEEE International Solid-State Circuits Conference · Feb 1, 2010

Show publication

The 32 nm implementation of an AMD x86-64 core occupying 9.69 mm2 and containing more than 35 million transistors (excluding L2 cache), operates at...

Other authors

+4

A 7th-generation x86 microprocessor

IEEE International Solid-State Circuits Conference · Feb 1, 1999

Show publication

The AMD-K7 (TM) processor is an out-of-order, three-way superscalar x86 microprocessor with a 15-stage pipeline, organized to allow 500+MHz operation. T...

Other authors

+7

Patents

Method and apparatus to achieve more level thermal gradient

US 7,991,955 · Issued Aug 2, 2011

See patent

Achieving better uniformity of temperature on an integrated circuit while performing burn-in can result in reduced burn-in time and more uniform acceleration. One way...

Other inventors

Memory array with global bitline domino read/write scheme

US 7,355,881 · Issued Apr 8, 2008

See patent

A circuit for implementing memory arrays using a global bitline domino read/write scheme. The memory circuit includes a plurality of cells each configured to store a b...

Other inventors

Integrated processor and memory control unit including refresh queue logic for refreshing DRAM during idle cycles.

US 5,873,114 · Issued Feb 16, 1999

See patent

An integrated processor is provided with a memory control unit having refresh queue logic for refreshing dynamic random access memory (DRAM) banks during idle...

Other inventors

Show all 8 patents →

Languages

English

Native or bilingual proficiency

Spanish

Native or bilingual proficiency

Interests

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Incoming CEO of Future Plc. Founder of Cheddar, former President/COO of BuzzFeed, former President News and Advertising at Altice USA
1,853,155 followers
+ Follow

Jeff Haden · 3rd
Speaker, Inc. Magazine contributing editor, author of THE MOTIVATION MYTH, ghostwriter.
1,056,738 followers
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Emily Slagle
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Marketing and Communications Coordinator at Robins Kaplan LLP

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Marc Betinsky
Partner at Robins Kaplan LLP

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Katie Bennett
Partner at Robins Kaplan LLP

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Ricardo Ehramjian
Senior A/V Engineer, Trial Consultant and Multimedia Expert at Robins Kaplan LLP

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